IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) An integrated circuit structure comprising:

a chip-level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip-level TAP controller,

wherein said embedded TAPs have ~~varying~~ instruction register lengths that differ from said chip-level TAP instruction register, ~~and~~

wherein said chip-level TAP instruction register comprises a flexible length instruction register,

wherein said flexible length instruction register comprises a plurality of instruction register segments,

wherein at least two of said instruction register segments comprise multiple bits, and

wherein said flexible length instruction register is adapted to accommodate different length instruction registers of said embedded TAPs.

2. (Previously Presented) The integrated circuit structure of claim 1, wherein said flexible length instruction register is longer than a longest embedded TAP instruction register.

3. (Previously Presented) The integrated circuit structure of claim 2,

wherein said flexible length instruction register further comprises additional bit segments,

wherein all of said instruction register segments combined are as long as said longest embedded TAP instruction register,

wherein said additional bit segments make said flexible length instruction register longer than said longest embedded TAP instruction register, and

wherein said additional bit segments comprise bits that are adapted to choose an effective length of said flexible length instruction register.

4. (Previously Presented) The integrated circuit structure in claim 3, wherein said plurality of instruction register segments comprise:

a first instruction register segment having a same length as a shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to a difference between said shortest embedded TAP instruction register and a next longer embedded-TAP instruction register.

5. (Previously Presented) The integrated circuit structure in claim 3, wherein said plurality of instruction register segments comprises:

a first instruction register segment having a same length as a shortest embedded TAP instruction register; and

at least two other instruction register segments having lengths equal to a difference between a previous shorter embedded TAP instruction register and a next-longer embedded TAP instruction register.

6. (Previously Presented) The integrated circuit structure in claim 5, further comprising a selection logic connected to each of said instruction register segments and to said additional bit segments, wherein said selection logic comprises a plurality of multiplexors adapted to selectively include with said first instruction register segment incremental ones of said instruction register segments to incrementally match a difference in length between longer embedded TAP instruction registers and said first instruction register segment.

7. (Previously Presented) The integrated circuit structure in claim 5, wherein said effective length of said flexible length instruction register comprises a combined length of said first

instruction register segment and selected ones of said at least two other instruction registers segments.

8. (Currently Amended) The integrated circuit structure in claim 1, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip-level TAP controller.

9. (Currently Amended) The integrated circuit structure in claim 1, further comprising a selection logic adapted to actively connect only a single embedded TAP at a time to said chip-level TAP controller.

10. (Currently Amended) An integrated circuit structure comprising:

a chip-level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip-level TAP controller,

wherein said embedded TAPs have instruction register lengths that differ from said chip-level TAP instruction register,

wherein at least some of said embedded TAP instruction register lengths may differ from each other,

wherein said chip-level TAP instruction register comprises a flexible length instruction register,

wherein said flexible length instruction register is adapted to accommodate different length instruction registers of said embedded TAPs, and

wherein said flexible length instruction register comprises:

a plurality of instruction register segments at least two of which comprise multiple bits[[,]]; and

additional bit segments,

wherein said plurality of instruction register segments comprise:

a first instruction register segment having a same length as a shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to a difference between said shortest embedded TAP instruction register and a next longer embedded TAP instruction register,

wherein all of said instruction register segments combined are as long as a longest embedded TAP instruction register,

wherein said additional bit segments make said flexible length instruction register longer than said longest embedded TAP instruction register, and

wherein said additional bit segments comprise bits that are adapted to choose an effective length of said flexible length instruction register.

11-12 (Cancelled).

13. (Currently Amended) The integrated circuit structure in claim 10, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip-level TAP controller.

14. (Currently Amended) The integrated circuit structure in claim 10, further comprising a selection logic adapted to actively connect only a single embedded TAP at a time to said chip-level TAP controller.

15. (Currently Amended) An integrated circuit structure comprising:

a chip-level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip-level TAP controller,

wherein said embedded TAPs have instruction register lengths that differ from said chip-level TAP instruction register,

wherein at least some of the embedded TAP instruction register lengths ~~may~~ differ from each other,

wherein said chip-level TAP instruction register comprises a flexible length instruction register,

wherein said flexible length instruction register is adapted to accommodate different length instruction registers of said embedded TAPs,

wherein said flexible length instruction register comprises a plurality of instruction register segments having a combined length equal to a longest embedded TAP instruction register and additional bit segments such that said flexible length instruction register is longer than said longest embedded TAP instruction register,

wherein said plurality of instruction register segments comprise:

a first instruction register segment comprising multiple bits and having a same length as a shortest embedded TAP instruction register; and

at least two other instruction register segments having lengths equal to a difference between a previous shorter embedded TAP instruction register and a next-longer embedded TAP instruction register, wherein at least one of said at least two other instruction register segments comprises multiple bits.

16. (Cancelled).

17. (Currently Amended) The integrated circuit structure in claim [[16]] 15, wherein said additional bit segments are adapted to choose an effective length of said flexible length instruction register.

18. (Previously Presented) The integrated circuit structure in claim 15, further comprising a selection logic connected to each of said instruction register segments and to said additional bit segments, wherein said selection logic comprises a plurality of multiplexors adapted to selectively include with said first instruction register segment incremental ones of said

instruction register segments to incrementally match a difference in length between longer embedded TAPs instruction registers and said first instruction register segment.

19. (Previously Presented) The integrated circuit structure in claim 17, wherein said effective length of said flexible length instruction register comprises a combined length of said first instruction register segment and selected ones of said at least two other instruction register segments.

20. (Currently Amended) The integrated circuit structure in claim 15, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip-level TAP controller.

21. (Currently Amended) The integrated circuit structure in claim 15, further comprising a selection logic adapted to actively connect only a single embedded TAP at a time to said chip-level TAP controller.

22. (Currently Amended) An integrated circuit structure comprising:

a chip-level test access port (TAP) controller, having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip-level TAP controller,

wherein said embedded TAPs have instruction register lengths that differ from said chip-level TAP instruction register,

wherein at least some of the embedded TAP instruction register lengths may differ from each other,

wherein said chip-level TAP instruction register comprises a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs,

wherein said flexible length instruction register comprises a plurality of instruction register segments having a combined length equal to a longest embedded TAP instruction

register and additional bit segments such that said flexible length instruction register is longer than the longest embedded TAP instruction register,

wherein said additional bit segments ~~that~~ are adapted to choose an effective length of said flexible length instruction register.

23. (Previously Presented) The integrated circuit structure in claim 22,

wherein at least two of said plurality of instruction register segments comprise multiple bits and

wherein said plurality of instruction register segments further comprise~~s~~:

a first instruction register segment having a same length as a shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to a difference between said shortest embedded TAP instruction register and a next longer embedded TAP instruction register.

24. (Previously Presented) The integrated circuit structure in claim 22, wherein said plurality of instruction register segments comprise~~s~~:

a first instruction register segment having the same length as a shortest embedded TAP instruction register; and

at least two other instruction register~~s~~ segments having lengths equal to a difference between a previous shorter embedded TAP instruction register and a next longer embedded TAP instruction register, wherein at least one of said at least two other instruction register segments comprises multiple bits.

25. (Previously Presented) The integrated circuit structure in claim 24, further comprising a selection logic connected to each of said instruction register segments and to said additional bit segments, wherein said selection logic comprises a plurality of multiplexors adapted to selectively include with said first instruction register segment incremental ones of said

instruction register segments to incrementally match a difference in length between longer embedded TAPs instruction registers and said first instruction register segment.

26. (Previously Presented) The integrated circuit structure in claim 24, wherein said effective length of said flexible length instruction register comprises a combined length of said first instruction register segment and selected ones of said at least two other instruction registers segments.

27. (Currently Amended) The integrated circuit structure in claim 22, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip-level TAP controller.

28. (Currently Amended) The integrated circuit structure in claim 22, further comprising a selection logic adapted to actively connect only a single embedded TAP at a time to said chip-level TAP controller.

29. (Original) The integrated circuit structure in claim 22, wherein said embedded TAPs comprise serially connected TAPs.

30. (Previously Presented) The integrated circuit structure in claim 22, wherein a number of said embedded TAPs is unlimited.